Electronic Version
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Claims

[c1] What is claimed is:

1.A reticle alignment procedure employed on a semiconductor wafer, a surface of the semiconductor wafer comprising a cell pattern area and a minor pattern area, the minor pattern area comprising at least one pre-layer wafer alignment mark (pre-layer wafer AM) transferred onto the semiconductor wafer from a pre-layer reticle alignment mark (pre-layer reticle AM) on a pre-layer reticle, the reticle alignment procedure comprising:

providing a current-layer reticle, the current-layer reticle comprising at least one current-layer reticle alignment mark (current-layer reticle AM) and a circuit pattern;

performing a baseline check (BCHK) to align the current-layer reticle AM with the pre-layer wafer AM;

capturing and comparing image signals of the current-layer reticle AM and the pre-layer wafer AM to calibrate a corresponding coordinate of the current-layer reticle to the semiconductor wafer;and

performing a lithography process to simultaneously transfer layouts of the circuit pattern and the current-layer reticle AM onto the semiconductor wafer to form a current-layer wafer alignment mark (current-layer wafer

AM) within the minor pattern area of the semiconductor wafer corresponding to the current-layer reticle alignment mark.

[c2] 2.The reticle alignment procedure of claim 1 wherein the minor pattern area is within a scribe line area.

[c3] 3.The reticle alignment procedure of claim 1 wherein images of the alignment marks are produced by utilizing a video reticle sensor (VRA sensor) of a reticle alignment machine.

[c4] 4.The reticle alignment procedure of claim 1 wherein a high-speed image processor is employed to capture, transfer, and store images of the alignment marks.

[c5] 5.The reticle alignment procedure of claim 3 wherein the VRA sensor utilizes a charge couple device camera (CCD camera) to capture images of the alignment marks.

[c6] 6.A method of utilizing a reticle alignment machine to calibrate a corresponding coordinate of a reticle to a semiconductor wafer during a plurality of lithography processes, the plurality of lithography processes comprising at least a first lithography process and a second lithography process performed by utilizing a first reticle and a second reticle, respectively, a surface of the semiconductor wafer comprising a cell pattern area and a mi-

nor pattern area, the minor pattern area comprising at least a first on-wafer alignment mark (first on-wafer AM), the first reticle comprising at least a first reticle alignment mark and a first circuit pattern, the second reticle comprising at least a second reticle alignment mark and a second circuit pattern, the method comprising:

providing the first reticle;

performing a baseline check to align the first reticle alignment mark on the first reticle with the first on-wafer alignment mark;

capturing and comparing image signals of the first reticle AM and the first on-wafer AM to calibrate a corresponding coordinate of the first reticle to the semiconductor wafer;

performing the first lithography process to simultaneously transfer layouts of the first circuit pattern and the first reticle alignment mark onto the semiconductor wafer to form a second on-wafer alignment mark (second on-wafer AM) within the minor pattern area of the semiconductor wafer, the second on-wafer alignment mark being a combination of the first on-wafer alignment mark and the first reticle alignment mark;

providing the second reticle;

performing a baseline check to align the second reticle alignment mark on the second reticle with the second

on-wafer alignment mark;

capturing and comparing image signals of the second reticle AM and the second on-wafer AM to calibrate a corresponding coordinate of the second reticle to the semiconductor wafer; and

performing a second lithography process to simultaneously transfer layouts of the second circuit pattern and the second reticle alignment mark onto the semiconductor wafer to form a third on-wafer alignment mark (third on-wafer AM) within the minor pattern area of the semiconductor wafer, the third on-wafer alignment mark being a combination of the second on-wafer alignment mark and the second reticle alignment mark.

[c7] 7.The method of claim 6 wherein the minor pattern area is within a scribe line area.

[c8] 8.The method of claim 6 wherein a high-speed image processor is employed to capture, transfer, and store images of the alignment marks.

[c9] 9.The method of claim 6 wherein the reticle alignment machine comprises a VRA sensor for producing images of the alignment marks.

[c10] 10.The method of claim 9 wherein the VRA sensor utilizes a CCD camera to capture images of the alignment

marks.